In the Claims:

Please amend the claims as indicated below.

1. (Currently Amended) An arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device, comprising:

a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal, said plurality of semiconductor switches being separated into groups of semiconductor switches and said groups of semiconductor switches being separated into subgroups of semiconductor switches;

a control bus having a plurality of conductors, each conductor being coupled to said first terminal of respective ones of each of said plurality of semiconductor switches for communicating corresponding signals; and ~~characterized by~~

a plurality of local buses that are separated from one another for communicating corresponding signals, ~~a given one~~ each of said plurality of local buses being associated with a respective group of semiconductor switches and having a plurality of conductors, each of said plurality of conductors having a first bus section ~~coupled to said second terminal of respective ones of said plurality of semiconductor switches, each said first bus section~~ extending in a manner to cross said plurality of conductors of said control bus once and a second bus section connected to an end of said first bus section and ~~having conductors thereof~~ coupled in a local, clustering bus arrangement to the second ~~terminals~~ terminal of ~~the~~ a respective ~~ones of said plurality of switches~~ semiconductor switch within each subgroup of the respective group of semiconductor switches, the associated switches having the third terminals thereof coupled to the consecutively disposed column conductors of the array of the display device.

2. (Previously Amended) An arrangement according to Claim 1 wherein said first plurality of terminals receive switch control signals and said second plurality of terminals receive picture information signals for said switches for storing the picture information in said pixels of said array.

3. (Previously Amended) An arrangement according to Claim 1, wherein said associated switches including a plurality of sub-groups of switches, the switches of a given sub-group having the first terminals thereof coupled in common to a corresponding conductor of said first bus and the third terminals thereof being coupled to consecutively disposed column conductors, respectively, of said array.

4. (Previously Amended) An arrangement according to Claim 1, wherein the conductors of said second bus section of said given local bus are disposed proximate said switches associated with said given bus and remote from switches associated with the other local buses of said plurality of local buses to provide bus separation.

5. (Previously Amended) An arrangement according to Claim 1, wherein the conductors of said first bus extend along each of said plurality of semiconductor switches to form a global bus arrangement.

6. (Previously Amended) An arrangement according to Claim 1, wherein said third terminal of each of said semiconductor switches is coupled to an input terminal of a corresponding data line driver.

7. (Currently Amended) A signal demultiplexer for a display panel, comprising:

a plurality of switch groups, each switch group including a plurality of subgroups, each subgroup having ordinally numbered switches 1 thru n arranged sequentially, and each switch having respective input, output and control terminals with the control terminals of all switches in each ~~group~~ subgroup being connected to a common control terminal, and having respective output terminals coupled to successive data lines on the display panel;

a plurality of groups of data buses, each group of data buses being associated with a respective switch group and having ordinally numbered conductors 1 thru n, the ordinally numbered conductors of respective groups of data buses being coupled to input terminals of a corresponding ordinally numbered ~~switches~~ switch of ~~a certain~~ each

subgroup within the respective switch ~~groups within said plurality of switch groups~~ group; characterized by

a control bus including a plurality of conductors, ~~said control bus arranged to cross~~ said plurality of groups of data buses having a first bus section extending in a manner to cross said plurality of conductors of said control bus once and a second bus section connected to an end of said first bus section and coupled in a local, clustering bus arrangement to the second terminal of a respective semiconductor switch within each subgroup of the respective group of semiconductor switches; and

connections between ones of said plurality of conductors of said control bus and ~~respective~~ a common control ~~terminals~~ terminal of a respective subgroup within each of said plurality of switch groups.

8. (Cancelled)

9. (Cancelled)